

Syna Gogte

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EDUCATION

University of Southern California

Los Angeles, CA

Master's & Bachelor's of Science — Computer Engineering and Computer Science

May 2026

Relevant HW Coursework: Digital Circuits, MOS VLSI Circuit Design, System on Chip Design, Computer Architecture, Hardware Foundations for ML, Introduction to Embedded Systems, Operating Systems, Algorithms, Linear Algebra, Probability

SKILLS

Languages: Python, C / C++, Java, Verilog, SystemVerilog, MATLAB, SQL

Tools & Frameworks: PyTorch, Arduino, ModelSim, Grafana, Git, GitHub, Linux, Figma

WORK EXPERIENCE

NVIDIA

Santa Clara, CA

Systems Software Engineering Intern

May 2025 – August 2025

- Implemented profile-guided optimizations improving execution speed by 20%, directly contributing to millions in annual revenue savings
- Developed a runtime tracing tool to aid debugging, reducing bug resolution time by 50% and accelerating development velocity

NVIDIA

Santa Clara, CA

System Software Engineering Intern

May 2024 – August 2024

- Enhanced coverage analysis tools by integrating Bullseye coverage data collection into GPU system processes (C), identifying 20% total code coverage
- Implemented and tested GSP-RM coverage collection and clearing functionalities, resulting in a 10% reduction in code bugs

USC ANRG — Autonomous Networks Research Group

Los Angeles, CA

Undergraduate Researcher

August 2024 – Present

- Implementing scheduling algorithms for conditional task graphs, targeting 20% reduction in total makespan vs. baseline algorithms

BMC Software

Santa Clara, CA

R&D Intern

May 2023 – November 2023

- Developed an internal chatbot via Flask API and Python; established POST call with confirmation flow, delivering high-quality production components

USC Viterbi School of Engineering

Los Angeles, CA

Course Producer — EE109 / EE250 / EE354 (Embedded Systems, Distributed Systems, Digital Circuits)

August 2023 – Present

- Guided instruction of C embedded software/hardware, Verilog, networking, and Python to 210+ students
- Conducted weekly labs, hosted office hours, and evaluated assignments to reinforce curriculum

PROJECTS

SqueezeNet Inference on FPGA

 Python · SystemVerilog · Quartus

- Implemented full SqueezeNet architecture for inference on an FPGA board including quantization and all modules
- Trained model in Python to obtain weights, then deployed quantized inference directly on hardware

Fine-tuning LLaMA 3.2-1B

 Python · PyTorch · LoRA

- Built a custom PyTorch pipeline with gradient accumulation, mixed precision, gradient checkpointing, and LoRA, reducing trainable parameters to 0.113% of the model
- Achieved >35% lower memory usage and 2x faster training on a single 16GB GPU while maintaining effective model convergence

CNN on FPGA

 Python · SystemVerilog · C · ModelSim

- Trained and tested CNN in Python; deployed forward pass in SystemVerilog supporting variable input sizes
- Used Nios II processor and C to compute weights after backpropagation; achieved ~80% accuracy on hardware

Connect 4 on FPGA

 Verilog · Python

- Designed RTL state machine logic in Verilog to emulate a full Connect 4 game on hardware
- Enhanced simulation accuracy and design verification across complete game logic

ACTIVITIES

HackSC Community Lead & HackerXP Member— Organized workshops, speakers, and events for USC's annual hackathon; brought together 500+ students